Name:_____

Reg No.:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN

Duration: 3 Hours

Max. Marks: 100

PART A

Answer all eight questions, each question carries 5 marks.

1. Why is two's - complement methodof representing signed integer numbers preferred over ones complement in digital circuits? What is range of numbers that can be represented using two complement with fourbits.
2. Expand$A + B\,\overline{C} + AB\,\overline{D} + ABCD$ to min-terms and max-terms
3. Obtain the logic function (based on the truth table) needed to implement a half adder circuit using NAND logic.
4. Explain the functioning of Master-Slave J-K flip-flop.
5. Explain the working of Johnson counter.
6. What is meant by synchronous counter? Give an example
7. What is mean by programmable logic devices?
8. Differentiate DAC and ADC

PART B

Answer any two questions, each question carries 10 marks.

9. a. With examples, explain the conversion of a gray code to corresponding binary code sequence and vice-versa. (5)
   b. Reduce the expression f= πM(0,1,2,3,4,7) using K-maps and implement it using NOR logic (5)
10. a. How parity checkers help in finding errors in digital data transmission. (5)
    b. Differentiate the features of CMOS and TTL logic gates. (5)
11. a. With examples, explain the significanceof Octal number system and Hexadecimal number system in digital circuit designs. (4)
    b. Reduce the expression f = ∑ m (0,1,2,3,5,7,8,9,10,12,13) using K-maps and implement the real minimal expression using NAND logic (6)

PART C

Answer any two questions, each question carries 10 marks.

12. What is the purpose of decoder? Explain the functioning of a BCD to Decimal Decoder circuit (10)

13. a. Differentiate Multiplexer and De-multiplexer. With simple examples, explain how they are implemented. (5)
    b. Differentiate SR and JK flip-flops. (5)
14. With the help of neat circuit and timing diagram, explain the functioning of a BCD decade asynchronous counter (MOD10) (10)

PART D

Answer any two questions, each carries 10 marks.

15. Design a counter for the following irregular binary count sequence using J-K flip flops

    001→010→101→ 111 → 001(recycles) (10)

16. a. Draw the truth-table and logic circuit diagram of a Ring counter (5)
    b. What is the basic difference between PAL (programmable Array Logic) and PLA (Programmable Logic Array). (5)
17. Explain the working of
    (i) R-2R Ladder type DAC
    (ii) Successive approximation ADC (5+5)

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